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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,469	01/13/2004	Chen-Jung Tsai	0941-0895P	9925
2292	7590	09/16/2005	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/755,469

Applicant(s)

TSAI ET AL.

Examiner

Thao X. Le

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings were received on 09 Aug. 05. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6414385 to Huang et al.

Regarding claim 1, Huang discloses a semiconductor package structure in fig. 3-4 comprising: a chip 208, column 3 line 41, having an active surface 210a, column 3 line 42, and an opposing non-active surface 210b, wherein the active surface 210a consists of a central area and a peripheral area having a plurality of bonding pads 212, column 3 line 48, a lead frame 202, column 3 line 39, comprising a plurality of the leads 202, fig. 3, a plurality of tie bars 201, column 3 line 41, and a chip paddle 200, column 3 line 39, and attached to the active surface 210a of the chip 208, fig. 3-3A, in such a way as to avoid contact with the bonding pads 212, and a plurality of wires 216, column 3 line 53, electrically connecting the bonding pad 212 and the lead 202, fig. 3.

Regarding claim 2, Huang discloses the semiconductor package structure as claimed in claim 1, further comprising an encapsulation 218, fig. 3, covering the chip 208, the bonding pads 212, the chip paddle 200, the leads 202 and the wires 216, fig. 3.

Regarding claims 3, 6, 9, Huang discloses the semiconductor package structure as claimed in claim 1, wherein the chip paddle 200 and the active surface 210a of the chip 208 are connected by non-conductive solid or liquid glue 214, column 3 line 51.

Regarding claim 4, Huang discloses a semiconductor package structure in fig. 3-4 comprising: a chip 208, fig. 3, having an active surface 210a, and an opposing non-active surface 210b, wherein the active surface 210a consists of a central area and a peripheral area having a plurality of bonding pads 212, fig. 3, a lead frame 202 comprising a plurality of the leads 202, fig. 3, a plurality of tie bars 201, fig. 3A, and a chip paddle 200, the tie bars 201 connecting to the chip paddle 200 and attached to the active surface 210a of the chip 208, fig. 3-3A, in such a way as to avoid contact with the bonding pads 212, and each of the leads 202 comprising a wire-connecting surface (top) 206a, fig. 3, and a wire non-connecting surface (bottom) 206b, fig. 3, a plurality of wires 216, column 3 line 59, electrically connecting the bonding pad 212 and the wire-connecting surface 206a of the lead 202, fig. 3, and an encapsulation 218 covering the active surface 210a of the chip 208, the bonding pads 212, the chip paddle 200, the wire-connecting surface 206a of the leads 202, and the wires 216, such that the opposing non-active surface 210b of the chip 208 and the wire non-connecting surface 206b (bottom) of the lead 202 are thereby exposed, fig. 5.

Regarding claims 5, 8, Huang discloses the semiconductor package structure wherein the leads 202 further comprise a plurality of inner leads (where wire 216 is located) and outer leads covered by the encapsulation 218 and the outer leads extending beyond the encapsulation 208, fig. 3A.

Regarding claim 7, Huang discloses a semiconductor package structure in fig. 3 comprising: a chip 208, having an active surface 210a, fig. 3, and an opposing non-active surface 210b, wherein the active surface 210a consists of a central area and a peripheral area having a plurality of bonding pads 212, fig. 3, a lead frame 202 comprising a plurality of the leads 202, fig. 3, a plurality of tie bars 201, fig. 3A, and a chip paddle 200, fig. 3, having an adhering surface and an opposing non-adhering surface, the adhering surface is connected with the central area, fig. 3, the tie bars 201 connecting to the chip paddle 200 and attached to the active surface 210a of the chip 208, fig. 3-3A, in such a way as to avoid contact with the bonding pads 212, and each of the leads 202 comprising a wire-connecting surface (top) 206a, fig. 3, and a wire non-connecting surface (bottom 206b, fig. 3, a plurality of wires 216, electrically connecting the bonding pad 212 and the wire-connecting surface 226 of the lead 202, fig. 3, and an encapsulation 218 covering the active surface 210a of the chip 208, the bonding pads 212, the chip paddle 200, the wire-connecting surface 206a of the leads 202, and the wires 216, such that the opposing non-active surface 210b of the chip 208 and the opposing non-adhering surface of the chip paddle 200 and the wire non-connecting surface of the lead 202 are thereby exposed, fig. 5.

Regarding claims 10, 12, and 16, Huang discloses the structure wherein the chip paddle 200 is protruding from the leads 202, fig. 3.

Regarding claims 11, 13, and 17, Huang discloses the structure wherein the chip 208 is surrounded by the chip paddle 200 and the leads 202, fig. 3.

Regarding claims 14 and 18, Huang discloses the structure wherein the wire-connecting surface 206a and the wire non-connecting surface 206b of the leads 202 are opposing, fig. 3.

Regarding claims 15 and 19, Huang discloses the structure wherein the opposing non-active surface 210b of the chip 208 and the non-connecting surface (bottom) 206b of the leads 202 are exposed in the same surface of the encapsulation, fig. 5.

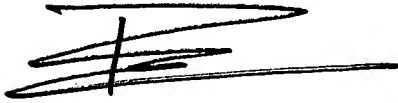
Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, consisting of several horizontal strokes and a vertical line intersecting them, located to the left of the printed name.

Thao X. Le
Patent Examiner
15 Sept. 2005

REPLACEMENT SHEET

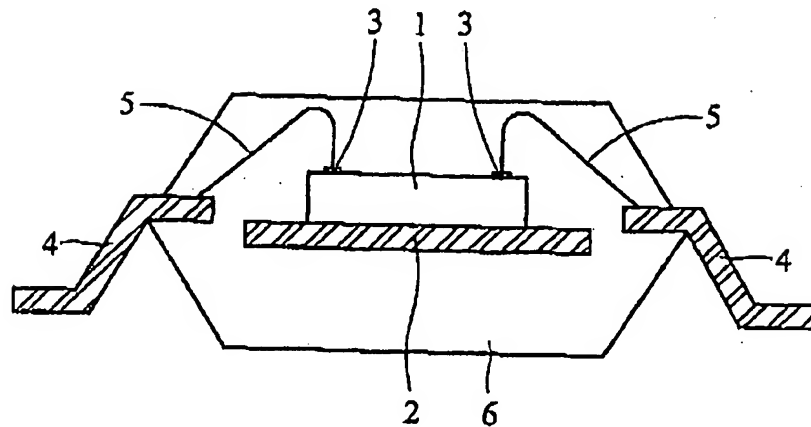


FIG. 1 (PRIOR ART)

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9/14/05

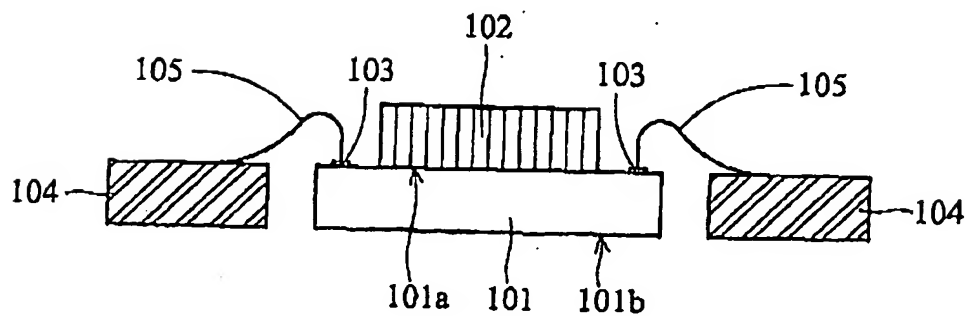


FIG. 2

REPLACEMENT SHEET

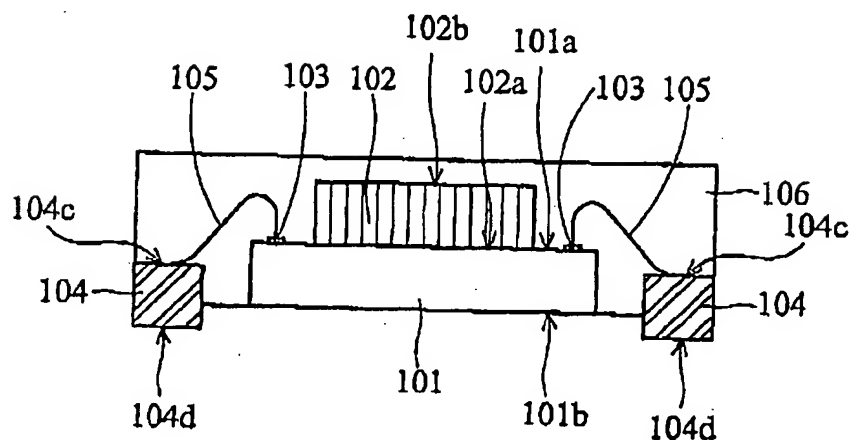


FIG. 5A

OK
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9/14/05

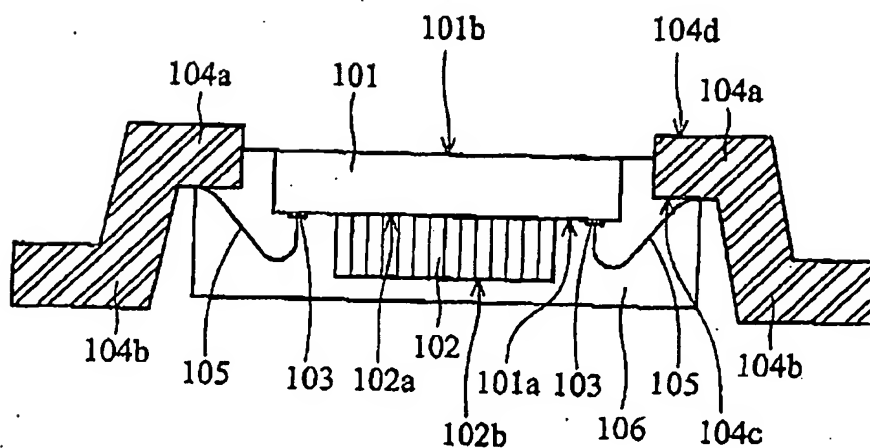


FIG. 5B